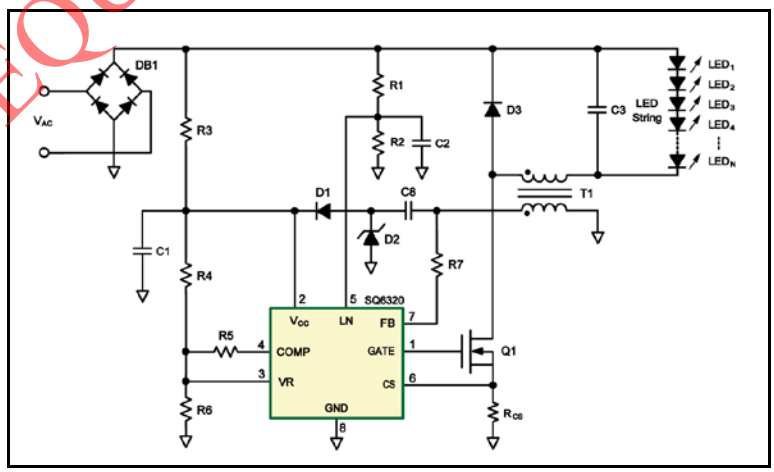
Features

- **Active power factor for $90V_{AC}$ to $130V_{AC}$ or $190V_{AC}$ to $265V_{AC}$**
- **Power Factor (PF) > 0.9**
- **Total Harmonic Distortion (THD) < 20%**
- **High efficiency up to 90%**
- **±3% output LED current accuracy**
- **Boundary conduction mode (BCM) operation**
- **Valley detection to turn on MOSFET to warrant the high efficiency switching**
- **Natural jittering operating frequency**
- **Excellent line regulation**
- **Low start up current (< 20μA)**
- **Low operating current (< 600μA)**
- **No input electrolytic capacitor**
- **Cycle-by-cycle current limiting**
- **Over/Under Voltage Protection (OVP/UVLO)**
- **LED Short Circuit Protection (SCP)**
- **Over Temperature Protection (OTP)**
- **Available in SOP-8 package**
- **RoHS compliant and Pb free**

Typical Applications

- **GU10/E26/E27 LED bulb lamps**
- **LED PAR30/PAR38 lamps**
- **T5/T8 LED light tubes**
- **External power supply for LED lights**

Typical Application Circuit



Product Description

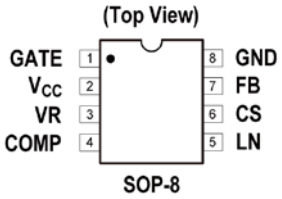
The SQ6320 is a high power factor constant current off-line LED controller with input voltage from $90V_{AC}$ ~ $130V_{AC}$ or $190V_{AC}$ to $265V_{AC}$ which is optimized for LED driver. The SQ6320 integrates a highly linear multiplier with THD optimizer for near unity power factor. The SQ6320 provides the most cost effective solution in non-isolated topology without input electrolytic capacitor. The SQ6320 operates in the boundary conduction mode with valley switching to detect the end of discharge at the output diode and turns on the external power MOSFET to ensure the highest efficiency without D3 diode reverse recovery and EMI problems.

The SQ6320 supports excellent line regulation by detecting average output current to achieve ±3% output current accuracy. The output current accuracy can be further improved with external circuit on CS pin through V_{CS} fold-back.

The SQ6320 has multiple-protections including short circuit protection, over voltage protection, under voltage protection, cycle-by-cycle current limiting, and over temperature protection. All protections have the automatic restart mechanisms. The SQ6320 is available in SOP-8 package.

For pricing, delivery, and ordering information, please contact Sequoia direct at 886-2-8780-8495, or e-mail to sales@sqme.com.tw or visit Sequoia's website at www.sqme.com.tw. This document contains information on a product under development. Sequoia reserves the right to change or discontinue this product without notice.

Pin Assignments and Ordering Information



Device	Packaging	Quantity of Tape & Reel
SQ6320 MST	SOP-8	3000

Pin Descriptions

Pin No.	Pin Name	Function
1	GATE	**Gate drive output pin**
		External power MOSFET gate drive.
2	V_{CC}	**Controller power input pin**
		Supply voltage for the controller.
3	VR	**Voltage reference sense pin**
		This pin is connected to an internal narrow bandwidth error amplifier to provide a reference for the multiplier.
4	COMP	**Loop compensation pin**
		A compensation capacitor is placed between this pin and GND to achieve stability of the voltage control loop and sets the internal error amplifier as a very narrow bandwidth low pass filter.
5	LN	**Linear voltage input pin**
		The voltage is used as the current reference for the PFC control.
6	CS	**Current sense pin**
		Senses current on external power MOSFET and compares it with sinusoidal input reference to determine when to turn off MOSFET to obtain high power factor. There is a 250ns leading edge blanking.
7	FB	**LED output current feedback sense pin**
		The voltage on this pin is used to detect the lowest point of the output discharging current.
8	GND	**Ground pin**
		Device ground.

Absolute Maximum Ratings (Note 1)

Symbol	Parametar	Ratings	Unit
V_{CC}	DC input supply voltage to GND	-0.3 ~ +26	V
V_{CS}	Current sense voltage range to GND	-0.3 ~ +8	V
V_{COMP}	Loop compensation voltage to GND	-0.3 ~ +8	V
V_{LN}	LN pin voltage range to GND	-0.3 ~ +8	V
V_{FB}	FB pin voltage range to GND	-0.3 ~ +8	V
$I_{CC(MAX)}$	V_{CC} pin maximum input current	+5	mA
$P_{D(MAX)}$	Continuous power dissipation (T_A = +25°C) (Note 2)		
	8 Pin SO (de-rating 6.3mW/°C above +25°C)	0.63	W
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	-55 ~ +150	°C
θ_{JA}	Junction-to-ambient thermal resistance	165	°C/W

Note :

1. Exceeding these ratings could cause damage to the device. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.
2. When the ambient temperature is high, the power dissipation has to decrease. It depends on T_{JMAX}, θ_{JA}, and the ambient T_A. The max. allowable power is $P_{D(MAX)} = (T_{JMAX} - T_A)/\theta_{JA}$, or the lower data in limit range.

Recommended Operating Conditions

Symbol	Parametar	Min.	Max.	Unit
V_{CC}	Power supply, V_{CC} to GND	11	22	V
V_R	VR pin voltage to GND	0	2.65	V
V_{LN}	LN pin voltage to GND	0	3	V
V_{CS}	CS pin voltage to GND	0	1.2	V
T_A	Ambient temperature range (Note 3)	-40	+85	°C

Note :

3. Maximum ambient temperature range is limited by allowable power dissipation.

Electrical Characteristics

(Over recommended operating conditions unless otherwise specified. T_A = +25°C, V_{CC} = 14V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Power Supply						
Start up voltage	V_{ST}	11.5	12.5	13.5	V	
Start up hysteresis voltage	ΔV_{ST}	2.0	2.5	3.0	V	
Start up current	I_{ST}		25	50	μA	Before turn-on, V_{CC} = 11V
Start up time	t_{ST}	100		300	μs	
Operating voltage	V_{CC}	11		22	V	After turn-on
Operating current	I_{CC}		3.5	5.0	mA	f_{OP} = 60kHz
Loop Compensation						
V_R reference voltage	V_R	2.4	2.5	2.6	V	11V < V_{CC} < 22V
V_R bias current	I_R			-1	μA	V_R = 2.5V
COMP upper clamp voltage	$V_{COMP(HI)}$	5.5	5.7	6.0	V	I_{COMP} = 0.5mA (sourcing)
COMP lower clamp voltage	$V_{COMP(LO)}$	2.00	2.15	2.40	V	I_{COMP} = 0.5mA (sinking)
Error amplifier voltage gain	G_V	60	70	80	dB	Open loop
FB						
Zero current threshold	V_{FB}		0.7		V	V_{FB} falling
Hysteresis voltage	ΔV_{FB}		0.7		V	V_{FB} rising
FB upper clamp voltage	$V_{FB(HI)}$	5.5	6.0	6.5	V	I_{FB} = 2.5mA
FB lower clamp voltage	$V_{FB(LO)}$	-0.3	0	0.3	V	I_{FB} = -2.5mA
Minimum t_{OFF} time	t_{OFF}	3	4	5	μs	
Maximum time out	t_{OUT}	150	200	250	μs	V_{FB} = 0.4V
CS Current Sense						
Current sense reference voltage	V_{CS}	1.05	1.10	1.15	V	V_{LN} = 1.5V, V_{COMP} = 5.7V
CS input bias current	I_{CS}			-1	μA	V_{CS} = 0V
Leading edge blanking interval	$t_{CS(LEB)}$	200	250	300	ns	
Delay from CS trip to GATE low	t_{DELAY}		100	200	ns	
Input Linear Voltage						
LN pin voltage range	V_{LN}	0		3	V	
LN input bias current	I_{LN}			-1	μA	V_{LN} = 0 ~ 3V
Internal multiplier gain (Note 4)	K	0.35	0.40	0.45		V_{LN} = 1V, V_{COMP} = 4V
Gate Drive						
GATE low voltage	$V_{GATE(LO)}$		0.4	0.6	V	I_{SINK} = 100mA
GATE high voltage	$V_{GATE(HI)}$	9.8	10.0		V	I_{SOURCE} = 5mA

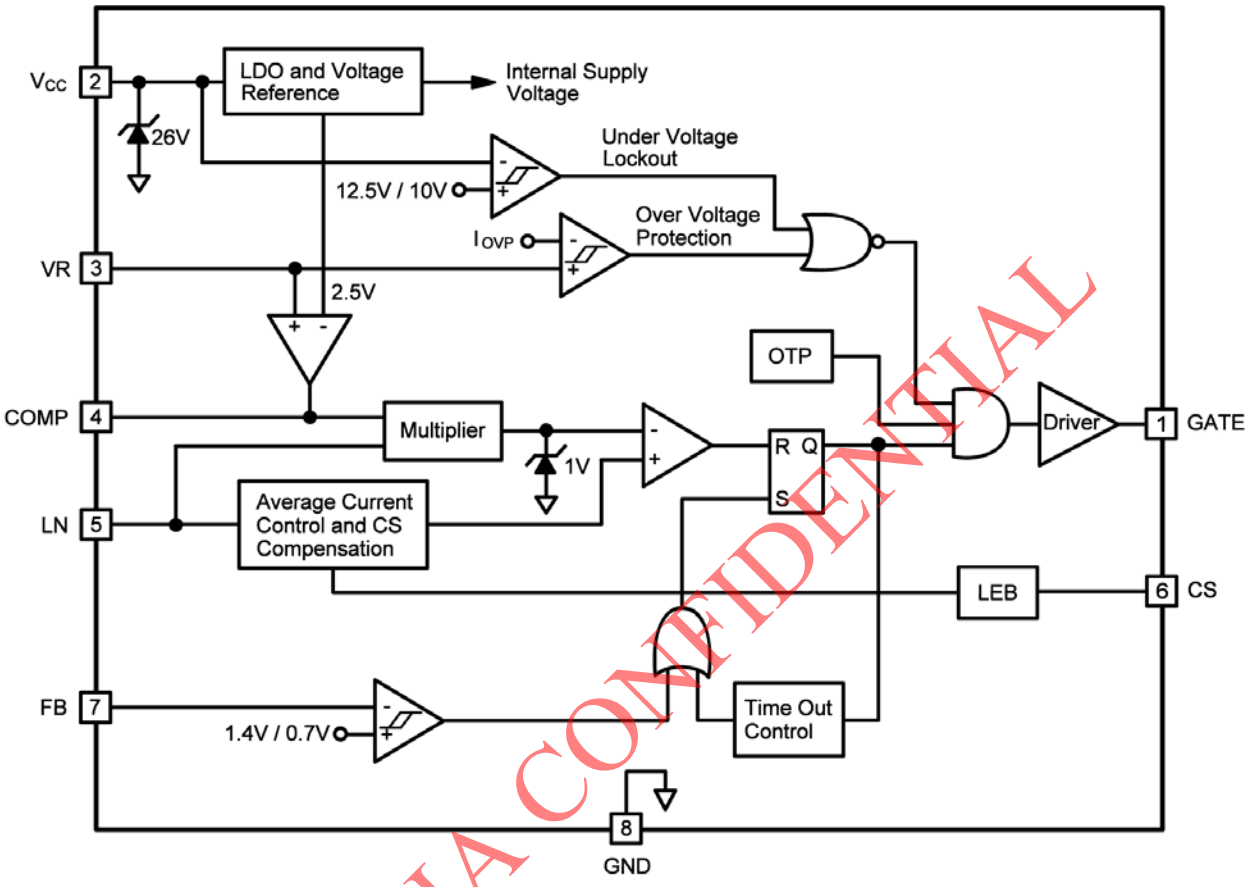
Electrical Characteristics (continued)

(Over recommended operating conditions unless otherwise specified. T_A = +25°C, V_{CC} = 14V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
GATE peak sourcing current	I_{SOURCE}	-0.7			A	
GATE peak sinking current	I_{SINK}	0.7			A	
Rise time	t_{RISE}		30	60	ns	
Fall time	t_{FALL}		20	50	ns	
Protection						
OVP triggering current at VR pin	I_{OVP}	23	27	32	μA	
OVP triggering current hysteresis at VR pin (Note 4)	ΔI_{OVP}		20		μA	
Thermal shut down	T_{SD}		150		°C	
Thermal shut down hysteresis	ΔT_{SD}		30		°C	

4. Parameters guaranteed by design, functionality tested in production.

Functional Block Diagram



Application Information

Function Description

The SQ6320 is a low cost, high power factor, constant current PWM driver IC for off-line LED lighting for input voltage range of $90V_{AC}$ to $130V_{AC}$ or $190V_{AC}$ to $265V_{AC}$. The SQ6320 uses a proprietary sinusoidal buck topology to achieve high power conversion efficiency, typically 0.85 or better.

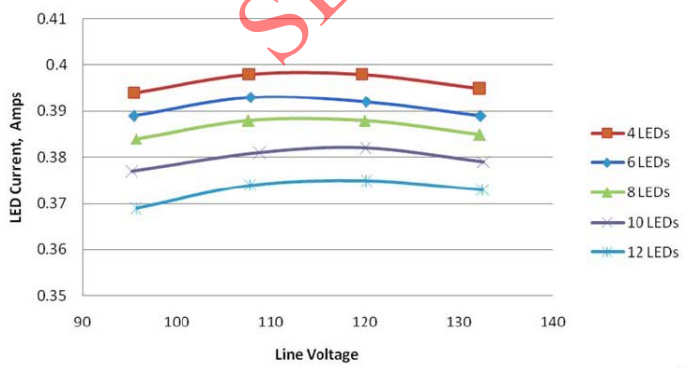
The SQ6320 also integrates active power factor function operating in transition mode (TM). This function allows SQ6320 easily to achieve PF > 0.9. The TM operation can reduce MOSFET switching loss to improve EMI performance and it also allows elimination of bulky input electrolytic capacitor.

Please refer to the application circuit in Figure 5; a high line regulation can be achieved by adding a filtered portion of the rectified AC line to compensate out the duty cycle shift due to line voltage. This is done through R11, R12, and R13 by adding compensation to the CS pin. Without these components, the SQ6320 will turn off MOSFET when it detects 1.1V at CS pin. With the compensation circuit, CS pin will drop about 0.6V at the current peak. The general line regulation can reach within 3% accuracy as shown in Figure 1.

Since the SQ6320 is used as buck converter, the efficiency is generally higher for more LEDs. Due to proprietary circuit, the efficiency of the circuit can achieve more than 85% for as few as only 6 LEDs.

The SQ6320 is offered in standard 8-pin SOIC package.

Figure 1. LED Current vs. Line Voltage



Start Up

At start up, the V_{CC} is lower than the V_{ST} threshold voltage, thus there is no gate pulse produced from the SQ6320 to drive the power MOSFET. Then the rectified AC voltage starts charging the capacitor C1 at V_{CC} pin through a start up resistor R3 to provide the start up current I_{ST} as shown in the Typical Application Circuit on page 1. Whenever the V_{CC} voltage is high enough to turn on the SQ6320 and generates the gate signal, the SQ6320 is operational and the supply current is switched to and provided from the auxiliary winding of T1 to enter the normal operation mode. From then on, the housekeeping power is supplied by the auxiliary (lower) winding. D1, D2 and C8 are used to detect the transitions on the auxiliary winding. D2 is a Zener diode, clamping the maximum voltage applied to C1 to slightly higher than 16V. Lower start up current can be achieved with larger R3 and it also reduces the power consumption on R3. The maximum start up current is less than 50μA. If a higher resistance value of R3 is selected, it usually takes longer time to start up. By carefully selecting the value of R3 and C1 can optimize the power consumption and start up time.

Setting Output Current

When the buck converter topology is selected, the peak CS voltage is a good representation of the average current in the LED. However, there is a certain error associated with this current sensing method that needs to be accounted for. This error is introduced by the difference between the peak and the average current in the inductor. For example, if the peak-to-peak ripple current in the inductor is 100mA, to get a 350mA LED current, the sensing resistor should be as follows :

$$R_{CS} = \frac{1.1V}{350mA + 0.5 \times 100mA} = 2.75\Omega \quad (1)$$

The SQ6320 detects the MOSFET current from the CS pin; this is for the cycle-by-cycle current limit. The maximum voltage threshold of the current sense pin is set at 1.1V. Therefore, the MOSFET peak current can be calculated as

$$I_P = \frac{1.1}{R_{CS}} \quad (2)$$

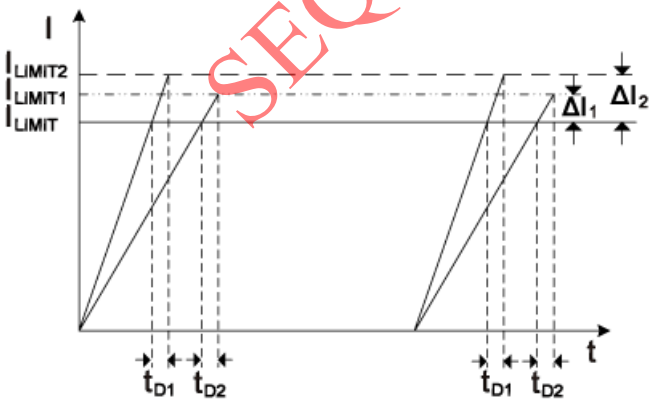
A 250ns leading edge blanking (LEB) time is included at the input of CS pin to prevent the false trigger from the current spike. In the low power application, if the total pulse width of the turn-on spike is less than 250ns and the negative spike on the CS pin does not exceed -0.3V, then, the RC filter can be eliminated. Please be noted that the total pulse width of the turn-on spike is decided by the power circuit design and the PCB layout. It is highly recommended to adopt a smaller RC filter for high power applications to avoid the CS pin being damaged by the negative turn-on spike.

However, during the MOSFET switching, there is a delay time due to the propagation delay from sensing the CS pin to the gate control circuit. This delay will lead to an error of the primary side peak current. This error increases with the input instantaneous line voltage increase.

As shown in Figure 2, ΔI_2 is bigger than ΔI_1 due to bigger rising slope (the higher the input voltage, the bigger the rising slope). Thus, the difference of ΔI will cause a bad output LED current line regulation.

The propagation delay influence to the line regulation can be improved by adding fold-back compensation to the CS pin from AC line voltage. The SQ6320 can increase the ON time of the power switch with a positive offset (feed-forward) added to the output of the multiplier near the voltage zero crossing at FB pin, and add a negative offset as the input line voltage increases. This is to achieve excellent line regulation over the operating voltage range. The higher line voltage, the higher fold-back offset.

Figure 2. Current Propagation Delay



Power Factor Control

PFC function is achieved by sampling the input sinusoid signal and compared with internal current requirement through a multiplier in transition mode operation.

The current requirement comes from CS pin. First, the sensed current will be fed to the control block to calculate its average value. The error amplifier compares the average value with the output of the multiplier which is clamped at 1V. The output of the comparator generates a signal error proportional to the difference between two values. If the bandwidth of the error amplifier is narrow enough, the error signal is literally a DC value and keeps at a constant value until the average value equals the reference from the output of the multiplier which sets the sinusoidal envelop.

The LN pin is one of the inputs of the internal multiplier. The output of the multiplier will be shaped as sinusoidal too. This signal is used as the reference for the current comparator with the current requirement from the CS pin which sets the primary peak current shaped as sinusoid in phase with the input line voltage cycle by cycle.

The LN pin's linear operation range is 0 ~ 3V. Be noted that the LN pin voltage needs to be set low enough at the minimum AC input so that the LN voltage will not exceed 3V at the maximum AC input. However, if the LN pin voltage is set too low, this will require a higher COMP voltage to regulate the same LED current and hence it may cause the COMP voltage to saturate. A recommended model to set the LN voltage can be set by the following equation :

$$V_{LN} = V_{IN(MAX)} \times \frac{R2}{R1+R2} \approx 3.0\,V \qquad (3)$$

where

$V_{IN(MAX)}$ is the maximum input peak voltage and equals to $V_{AC(MAX)} \times \sqrt{2}$.

Considering power loss, R1 should be chosen large enough, for example as 1MΩ and LN signal should be brought in before the EMI filter for better PF value.

An important advantage of the SQ6320 is that there is no need for large electrolytic or tantalum filter capacitor after the input bridge rectifier.

Usually, the conventional LED driver circuit requires an input capacitor of 2μF per watt. For SQ6320 systems, it only requires a very small input filter capacitor about 0.33μF (C4) if a high frequency switching noise needed to be blocked from injecting into AC lines or an EMI π filter can be used if a better EMI reduction is required.

Valley Switching

Zero current detection at FB pin is very critical to ensure that SQ6320 operates in transition mode. Please refer to the Typical Application Circuit on page 1; after the MOSFET turns off, the current in the upper winding of T1 continues to flow, instead, now it flows through D3 and the current ramps towards zero as it discharges the energy through the LEDs. When D3 turns off, the upper winding inductance of T1 and its parasitic capacitance then ring the voltage at D3's anode down to about twice the LED voltage below the positive V_{IN} power rail. When the ringing voltage turns up, the FB pin detects the end of discharge which is valley of the parasitic resonance and turns on the MOSFET. The cycle then repeats. Current in T1's upper winding therefore ramps between zero and twice the load current. When MOSFET turns on again in a new cycle, D3 has already turns off, thus, the MOSFET does not see D3's reverse recovery spike.

This operation produces a constant ON-time over each line half-cycle as below :

$$V_{CS} = R_{CS} \times V_{IN} \times (t_{ON} / L_M) \quad (4)$$

$$V_{LN} = K_1 \times K_2 \times V_{IN} \times V_{COMP} \quad (5)$$

If $V_{CS} = V_{LN}$ as the input current reaches the sinusoid envelop, then we get

$$t_{ON} = L_P \times K_1 \times K_2 \times V_{COMP} / R_{CS} \quad (6)$$

where

L_M is the inductance of the upper winding of T1.

R_{CS} is the current sense resistor.

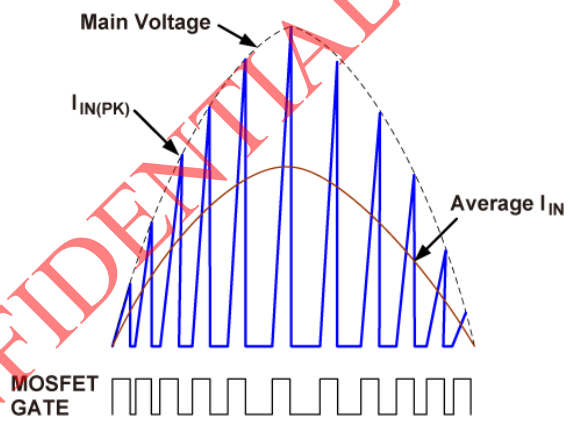
K_1 is the multiplier gain.

K_2 is the voltage scaling factor at LN pin.

There is a 200μs time-out to generate a MOSFET turn on signal if the ringing voltage stays low for more than 200μs.

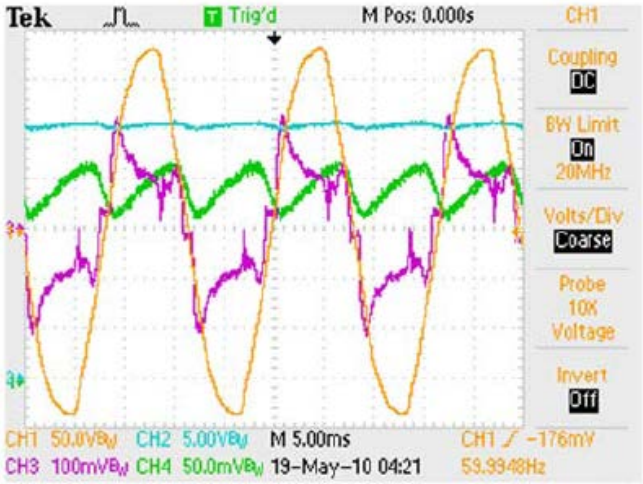
Since the SQ6320 operates in transition constant t_{ON} mode, due to variable t_{OFF} time, the switching frequency is naturally modulated as V_{IN} varies and it follows the AC line's sinusoidal waveform. This creates a natural frequency jittering which helps the LED lighting fixture to meet the EMI compatibility requirement. The currents at the input current and the MOSFET gate waveforms are shown in Figure 3.

Figure 3. Input Current and GATE Waveforms



The resultant input and output voltages and currents are shown in Figure 4.

Figure 4. Input and Output Voltage/Current



where

Yellow : Line voltage

Magenta : Line current

Blue : LED voltage

Green : LED current

Protection Functions

The SQ6320 has multiple protection functions to increase the system reliability. The Over Voltage Protection (OVP) can be achieved through VR pin. If the current entering the VR pin is higher than the I_{OVP} threshold current of 27μA, the OVP is triggered and the output gate drive will turn off the power MOSFET. There is a 20μA hysteresis to turn on the internal circuit and start switching the MOSFET again. An advantage of using this technique is that the over voltage level can be set independently from the regulated output voltage.

An UVLO comparator is implemented in the SQ6320 to detect the voltage on the V_{CC} pin. It would assure that the supply voltage is high enough to power the chip. A hysteresis of 2.5V is to prevent the shut down from the voltage dip during soft start. The turn-on and turn-off threshold levels are set at 12.5V and 10V, respectively.

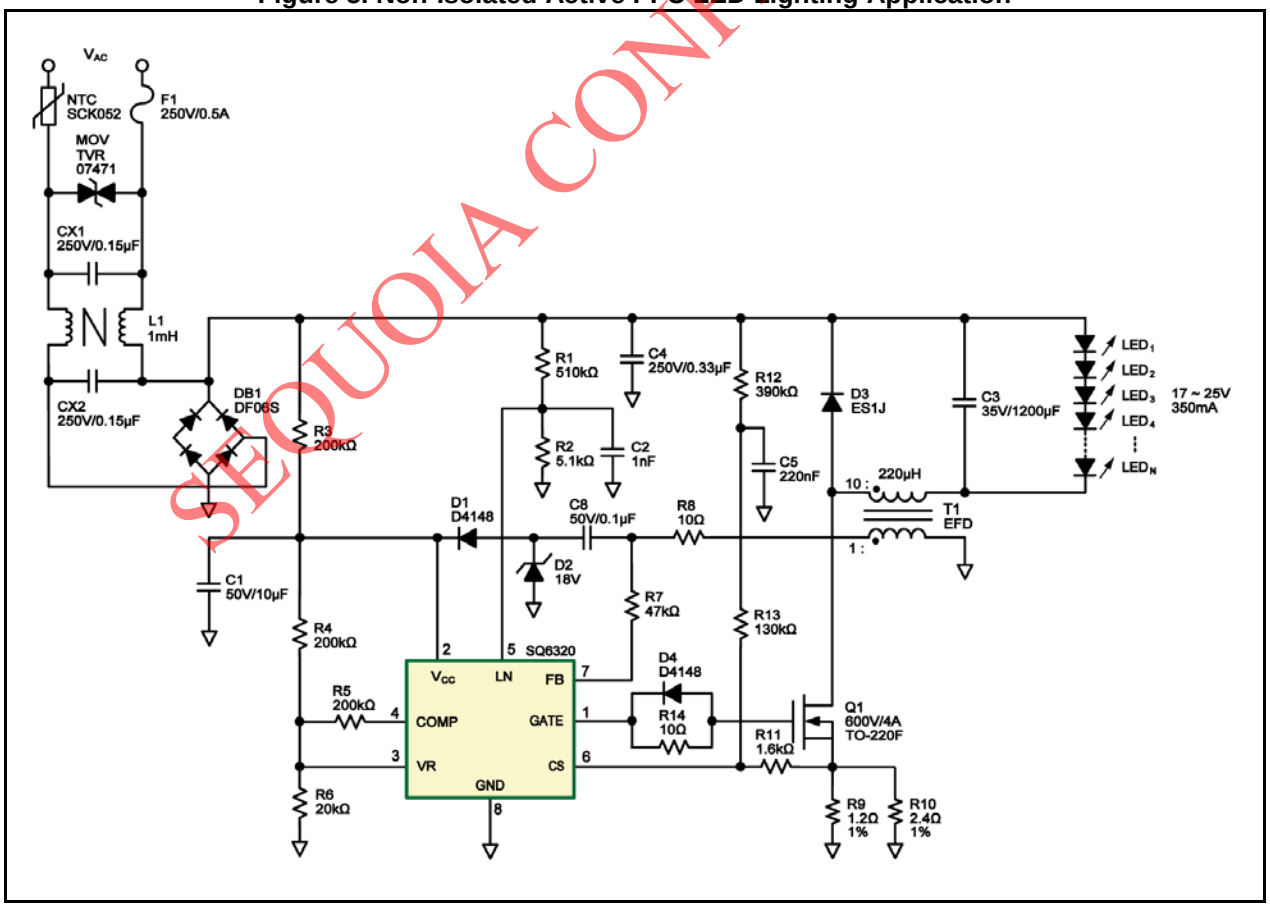
When output LED short occurs; the lower winding of T1 inductor will incur a voltage drop. As FB pin detects the drop below 0.7V, the external MOSFET is turned on until V_{CS} rises to 1V, then the MOSFET is turned off. The cycle starts again repeatedly.

The circuit shown in Figure 5 cannot provide output Open Loop Protection (OLP) because monitoring the voltage on C1 does not provide an indication of the output voltage.

The SQ6320 has built-in over temperature protection for junction temperature set at 150°C. There is a typical 30°C hysteresis. The controller auto re-starts operating when temperature drops more than 30°C.

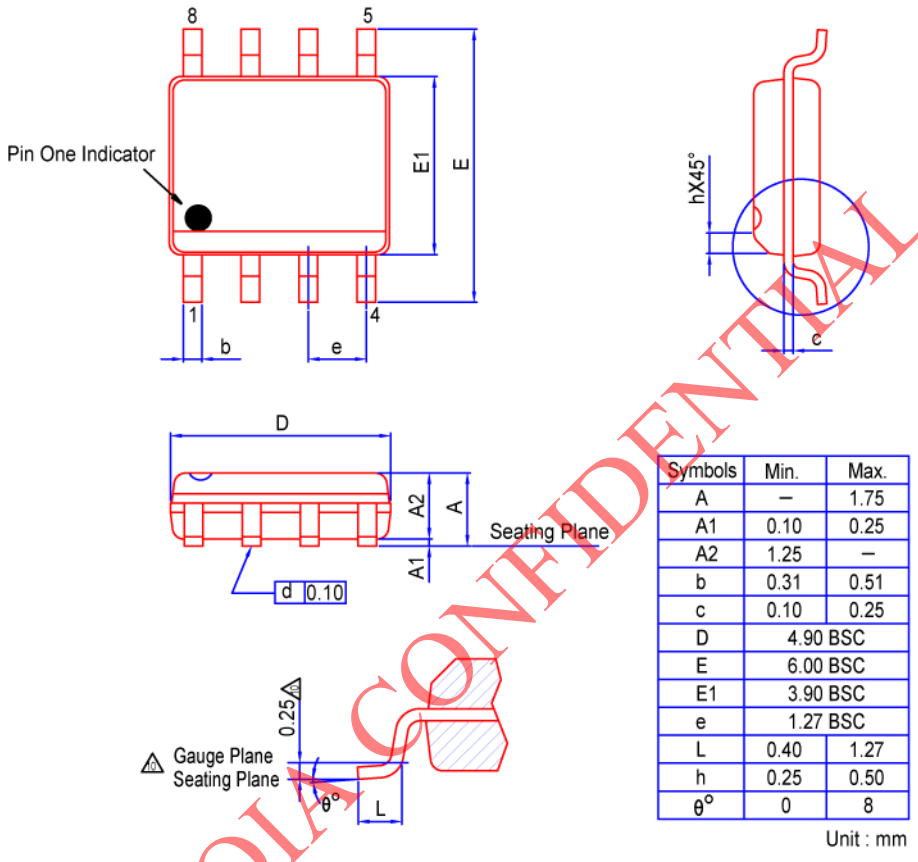
An example application circuit with SQ6320 is shown in Figure 5.

Figure 5. Non-Isolated Active PFC LED Lighting Application



Package Outline Dimensions

Package Type : SOP-8

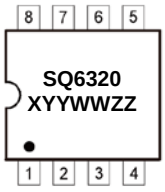


Symbols	Min.	Max.
A	–	1.75
A1	0.10	0.25
A2	1.25	–
b	0.31	0.51
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

Unit : mm

Marking Information

SOP-8



X = A/T Site, YY = Year, WW = Working Week, ZZ = Device Version

Sequoia Microelectronics Corp. (**Sequoia**) reserves the right to make changes to its data sheets and/or products or to discontinue any integrated circuit product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current and complete. Any products are sold subject to the terms and conditions of sales supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement and limitation of liability.

Sequoia warrants performance of its products to the specifications applicable at the time of sales in accordance with **Sequoia**'s standard warranty. Testing and other quality control techniques are utilized to the extent **Sequoia** deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customer acknowledges that **Sequoia** products are not designed, manufactured, intended, authorized, or warranted to be suitable for use in any systems or products intended for use in connection with life support or other hazardous activities or environments in which the failure of the **Sequoia** products could involve potential risks of death, personal injury, or severe property or environmental damage ("High Risk Activities"). **Sequoia** hereby disclaims all warranties, and **Sequoia** will have no liabilities to customer or any third party, relating to the use of **Sequoia**'s products in connection with any high risk activities.

Any support, assistance, recommendation or information that **Sequoia** may provide to customer (including, without limitation, regarding the design, development or debugging of customer circuit board or other application) is provide "AS IS". **Sequoia** does not make, and hereby disclaims, any warranties regarding any such support, including, without limitation, any warranties of merchantability or fitness for a particular purpose, and any warranty that such support will be accurate or error free or that customer circuit board or other application will be operational or functional. **Sequoia** will have no liability to customer under any legal theory in connection with customer use of or reliance on such support.

Sequoia cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a **Sequoia** product. No circuit patent licenses are implied. **Sequoia** reserves the right to change the circuitry and specifications without notice at any time.